UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,434	12/13/2001	Bradley J. Howard	97-0008.01	7606

7590 11/17/2004

Richard D. Egan
O'KEEFE, EGAN & PETERMAN
Building C, Suite 200
1101 Capital of Texas Highway South
Austin, TX 78746

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,434	HOWARD, BRADLEY J.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8-10,19,21-24,34-37 and 49-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8-10,19,21-24,34-37 and 49-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 6 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Naik et al. (U.S. Pub. 2003/0062627).

In re claim 6, **Naik** discloses a semiconductor device formed using a photo-definable layer **(FIG. 4E: 408)** in a positive mask scheme (page 3, paragraphs [0023]-[0024]), comprising (pages 5-6, paragraphs [0053]-:[0059] and **FIGS. 1A-4J**): a substrate **(FIG. 4E: 400)**; at least one feature formed on the substrate by converting selected portion of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation **(FIG. 4E: 418)** (page 5, paragraph [0055]) in a positive mask scheme and by using non-exposed portions **(FIG. 4E: 424)** (page 5, paragraph [0055]) of the photo-definable layer as a mask to form at least one feature **(FIGS. 4G-J: 426, 430)** (pages 5-6, paragraph [0058]); and an insulative layer formed on the substrate from the non-exposed portion **(FIG. 4E: 424)** of the photo-definable layer **(FIG. 4E: 408)** which remain after the positive mask scheme and are then subsequently converted to an

insulative layer through exposure to electro-magnetic radiation **(FIG. 4E: 418)** (page 5, paragraphs [0053]-[0057]).

In re claim 8, **Naik** discloses wherein the photo-definable layer comprises an organosilicon resist (page 5, paragraph [0053]).

In re claim 9, **Naik** discloses wherein the photo-definable layer comprises plasma polymerized methylsilane (PPMS) (page 5, paragraph [0053]).

In re claim 10, **Naik** discloses wherein the feature is part of a memory cell array (pages 5-6, paragraph [0058]).

2. Claims 19 and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Naik et al. (U.S. Pub. 2003/0062627).

In re claim 19, **Naik** discloses a patterned insulative structure within a semiconductor device formed using a photo-definable layer **(FIG. 4E: 408)** in a positive mask scheme (page 3, paragraphs [0023]-[0024]), comprising (pages 5-6, paragraphs [0053]-[0059] and **FIGS. 1A-4J**): a substrate **(FIG. 4E: 400)**; a patterned insulative layer formed on the substrate by converting selected portion of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation **(FIG. 4E: 418)** (page 5, paragraph [0055]) in a positive mask scheme and by using non-exposed portions **(FIG. 4E: 424)** (page 5, paragraph [0055]) of the photo-definable layer as a mask to form the patterned insulative layer wherein the insulative layer comprises an oxide layer and the non-exposed portions of the photo-definable layer are utilized to mask the oxide layer to form the patterned insulative layer (page 5, paragraph [0053]).

In re claim 21, **Naik** discloses wherein the photo-definable layer comprises an organosilicon resist (page 5, paragraph [0053]).

In re claim 22, **Naik** discloses wherein the photo-definable layer comprises plasma polymerized methylsilane (PPMS) (page 5, paragraph [0053]).

In re claim 23, **Naik** discloses wherein the insulative layer comprises a plurality of trench structures **(FIGS. 4G-J: 426, 430)** (pages 5-6, paragraph [0058]) within a memory cell array (pages 5-6, paragraph [0058]).

In re claim 24, **Naik** discloses wherein the patterned insulative layer comprises non-exposed portions **(FIG. 4E: 424)** of the photo-definable layer **(FIG. 4E: 408)** that were converted into additional insulative material after formation of the patterned insulative layer.

3. Claims 34-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Naik et al. (U.S. Pub. 2003/0062627).

In re claim 34, **Naik** discloses a conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising (pages 5-6, paragraphs [0053]-[0059] and **FIGS. 1A-4J**): a substrate **(FIG. 3H: 300)**; a first conductive layer **(FIG. 3H: 302)** over said substrate; an insulative layer **(FIG. 3H: 316)** over the conductive layer; and a second conductive layer **(FIG. 3I: 324)** formed within a desired portion of the insulative layer to create a conductive interconnect structure **(FIGS. 3A-I: 310, 320)** connected to the first conductive layer, the second conductive layer being formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation **(FIG. 4E: 418)** (page 5, paragraph [0055])

in a positive mask scheme, by using non-exposed portions **(FIG. 4E: 424)** (page 5, paragraph [0055]) of said photo-definable layer as a mask to form a pattern within the insulative layer, and by using non-exposed portions of said photo-definable layer as a sacrificial mask in etching the second conductive layer (pages 4-5, paragraphs [0045]-[0051] and **FIGS. 3A-I**).

In re claim 35, **Naik** discloses wherein the photo-definable layer comprises an organosilicon resist (page 5, paragraph [0053]).

In re claim 36, **Naik** discloses wherein the photo-definable layer comprises plasma polymerized methylsilane (PPMS) (page 5, paragraph [0053]).

In re claim 37, **Naik** discloses wherein the substrate includes a plurality of transistor gage structures for a memory cell array (pages 5-6, paragraph [0058]).

4. Claims 49-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Naik et al. (U.S. Pub. 2003/0062627).

In re claim 49, **Naik** discloses a pattern insulative structure within a semiconductor device using a photo-definable layer **(FIG. 4E: 408)** as a mask layer (page 3, paragraphs [0023]-[0024]), comprising (pages 5-6, paragraphs [0053]-:[0059] and **FIGS. 1A-4J**): a substrate **(FIG. 4E: 400)**; and an insulative layer on the substrate formed by covering a photo-definable layer with a separate patterned organic photoresist, by convering unmasked portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation **(FIG. 4E: 418)** (page 5, paragraph [0055]) and using non-exposed portions **(FIG. 4E: 424)** (page 5, paragraph [0055]) of the photo-definable layer

and organic photoresist as a mask to form a pattern within the insulative layer **(FIGS. 4G-J: 426, 430)** (pages 5-6, paragraph [0058]).

In re claim 50, **Naik** discloses wherein the photo-definable layer comprises an organosilicon resist (page 5, paragraph [0053]).

In re claim 51, **Naik** discloses wherein the photo-definable layer comprises plasma polymerized methylsilane (PPMS) (page 5, paragraph [0053]).

In re claim 52, **Naik** discloses wherein the insulative layer comprises an oxide layer (page 5, paragraph [0053]).

In re claim 53, **Naik** discloses wherein the insulative layer comprises a plurality of trench structures **(FIGS. 4G-J: 426, 430)** (pages 5-6, paragraph [0058]) within a memory cell array (pages 5-6, paragraph [0058]).

In re claim 54, **Naik** discloses wherein the insulative layer comprises non-exposed portions **(FIG. 4E: 424)** of the photo-definable layer **(FIG. 4E: 408)** subsequently converted into additional insulative material.

Response to Applicant's Amendment and Arguments

Applicant's arguments filed June 30th, 2004 have been fully considered but they are not persuasive.

Applicant contends that there is no disclosure in Naik (whether in the positive mask scheme or negative mask scheme) to utilize a process in which region of the photo-definable layer that remain after the mask scheme regions 408 are then subsequently converted to an insulative layer through exposure to further electro-magnetic ration.

In response to Applicant's contention that there is no disclosure in Naik (whether in the positive mask scheme or negative mask scheme) to utilize a process in which region of the photo-definable layer that remain after the mask scheme regions 408 are then subsequently converted to an insulative layer through exposure to further electro-magnetic ration, Examiner respectfully disagrees. Applicant is directed to (page 5, paragraphs [0053]-[0057]) where Naik discloses an insulative layer formed on the substrate from the non-exposed portion **(FIG. 4E: 424)** of the photo-definable layer **(FIG. 4E: 408)** which remain after the positive mask scheme and are then subsequently converted to an insulative layer through exposure to electro-magnetic radiation **(FIG. 4E: 418)**.

In response to Applicant's argument that Naik does not teach or suggest that the non-exposed portions of the photo-definable layer are utilized to mask the oxide layer to form the patterned insulative layer, Examiner respectfully disagrees. Applicant is directed to (page 5, paragraph [0053]) where Naik discloses that the non-exposed portions 424 of the photo-definable layer 408 are utilized to mask the oxide layer to form the patterned insulative layer (FIGS. 4E-I).

In response to Applicant's argument that nothing is pointed to Naik as disclosing the separate organic photoresist layer that covers the photo-definable layer, Examiner respectfully disagrees. Applicant is directed to (page 5, paragraphs [0054]-[0055]and FIG. 4E) where Naik discloses an insulative layer on the substrate 400 formed by covering a photo-definable layer 408 with a separate patterned organic photoresist by converting unmasked portions of a

photo-definable layer to an insulative material through exposure to electro-magnetic radiation 418 in a positive mask scheme.

For these reasons, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
November 12th, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER